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EXAMINER	
DUONG, FRANK	

ART UNIT	PAPER NUMBER
2666	

DATE MAILED: 03/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/023,971	KLAUSMEIER ET AL.	
	Examiner	Art Unit	
	Frank Duong	2666	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/17/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is a response to communications dated 12/17/01. Claims 16-33 are pending in the application.

Information Disclosure Statement

2. The information disclosure statement filed 12/17/01 complies with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609. It has been considered and placed in the application file.

Specification

3. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: "equations: 1) B<=N*T, wherein ... less than N*f", as recited in claim 27; "setting a value for N ... switch; setting a value B ... switch; setting a value T ... circuits; solving ... less than N*f", as recited in claims 32-33.

Claim Objections

4. Claim 28 objected to because of the following informalities: in accordance with the claim language, it should depend from claim 27. Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. Claims 27-30 and 32-33 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The rationales are as followings:

The claim limitations of "equations: 1) B<=N*T, wherein ... less than N*f", recited in claims 27-30 are not disclosed in the application. In the specification, on page 9, lines 5-18 and therein after, a feature designated as "*there are 384 outputs from each ... used as spares 780*" has been disclosed. From the disclosed feature, the claimed limitation of "equations: 1) B<=N*T, wherein ... less than N*f" cannot reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

The claimed limitations of "setting a value for N ... switch; setting a value B ... switch; setting a value T ... circuits; solving ... less than N*f", recited in the claims 32-33, are not disclosed in the application. In the specification, on page 9, lines 5-18 and therein after, a feature designated as "*there are 384 outputs from each ... used as spares 780*" has been disclosed. From the disclosed feature, the claimed limitation of "setting a value for N ... switch; setting a value B ... switch; setting a value T ... circuits; solving ... less than N*f" cannot reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

Double Patenting

6. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

7. Claims 16-24 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-8 of U.S. Patent No. 6,343,075.

'**971 application claim 16** calls for:

"A rearrangeable, non-blocking switch, comprising:

a first stage ***including*** *a plurality of first switch circuits, each of said plurality of first switch circuits including a plurality of inputs and a plurality of outputs;*

a second stage ***including*** *a plurality of second switch circuits, each of said plurality of second switch circuits including a plurality of inputs, each of which being respectively coupled to one of said plurality of outputs of each of said plurality of first switch circuits, and a plurality of outputs, a number of said plurality of second switch circuits equaling N, where N is an integer other than a power of 2; and*

a third stage ***including*** *a plurality of third switch circuits, each of said plurality of third switch circuits including a plurality of inputs and a plurality of outputs, each of said plurality of inputs of each of said plurality of third switch circuits being coupled to a respective one of said plurality of outputs of each of said plurality of second switch circuits,*

wherein at least some of said plurality of second switch circuits are each configured as a plurality of logical switch circuits."

'075 patent claim 1 calls for:

"A switch, comprising: a first stage having a plurality of first switch circuits, each of said plurality of first switch circuits having a plurality of inputs and a plurality of outputs;

a second stage ***having*** *a plurality of second switch circuits, each of said plurality of second switch circuits having a plurality of inputs, each of which being respectively coupled to one of said plurality of outputs of each of said plurality of first switch circuits, and a plurality of outputs, a number of said plurality of second switch circuits equaling N, where N is an integer other than a power of 2; and*

a third stage having a plurality of third switch circuits, each of said plurality of third switch circuits ***having*** *a plurality of inputs and a plurality of outputs, each of said plurality of inputs of each of said plurality of third switch circuits being coupled to a respective one of said plurality of outputs of each of said plurality of second switch circuits,*

wherein each of said plurality of outputs of said plurality of first switch

circuits, outputs of respective one of a plurality of data signals, said data signals being time-division multiplexed,

wherein said each of said plurality of data signals includes a plurality of groups of time slots, each of said plurality of groups further including a plurality of subgroups of time slots, and

wherein at least some of said plurality of second switch circuits are configured to be represented as n logical sub-switch circuits where n is a power of 2, each of said sub-switch circuits being configured to direct selected subgroups of time slots among different groups to one of said plurality of outputs of said plurality of second switch circuits."

Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following rationales:

First, the claimed invention of the instant application encompasses that of claims 1-8 of the '075 patent. Evidence can be found by comparing the claims 16-24 of the instant application with claims 1-8 of the '075 patent as shown above.

Second, claims 1-8 of patent '075 teach essentially the same limitations as claims 16-24 of the current application. Even though claims 16-24 are broadened by omitting certain limitations (i.e., the bolded texts shown above), it has been held that the omission of an element and its function is an obvious expedient if the remaining elements perform the same function as before. *In re Karlson*, 136 USPQ 184(CCPA).

Also note *Ex parte Rainu*, 168 USPQ 375 (Bd. App. 1969); omission of a reference element whose function is not needed would be an obvious variation.

Third, there is no apparent reason why applicant was prevented from presenting claims corresponding to those of the instant application during prosecution of the application which matured into a patent.

Claims 17-24 in the application defines an obvious variation of an invention claimed in the '075 patent for the same rationales discussed above.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 16-19, 23 and 25 are rejected under 35 U.S.C. 102(b) as being anticipated by Zola (USP 4,400,627) (hereinafter "Zola").

Regarding **claim 16**, in accordance with Zola reference entirety, Zola discloses a rearrangeable, non-blocking switch (Fig. 4), comprising:

a first stage (Input Stage Switches 101-164) including a plurality of first switch circuits (101-164), each of said plurality of first switch circuits including a plurality of inputs and a plurality of outputs (*see Fig. 4 for connections and description at col. 5, lines 33-43*);

a second stage (Center Stages Switches 201-203) including a plurality of second switch circuits (201-203), each of said plurality of second switch circuits including a plurality of inputs, each of which being respectively coupled to one of said plurality of outputs of each of said plurality of first switch circuits, and a plurality of outputs, a number of said plurality of second switch circuits equaling N, where N is an integer other than a power of 2 (*see Fig. 4 for connection and description at col. 5, lines 43-45. Three Center Stage Switches 201-203 are provides. Thus, three is not a power of 2*); and

a third stage (Output Stage Switches 301-364) including a plurality of third switch circuits, each of said plurality of third switch circuits including a plurality of inputs and a plurality of outputs, each of said plurality of inputs of each of said plurality of third switch circuits being coupled to a respective one of said plurality of outputs of each of said plurality of second switch circuits (*see Fig. 4 for connections and description at col. 5, lines 55-59*),

wherein at least some of said plurality of second switch circuits (201-203) are each configured as a plurality of logical switch circuits (*connection process of the switches is discussed at col. 5, line 60 col. 6, line 22*).

Regarding **claim 17**, in addition to features recited in base claim 16, Zola further discloses wherein at least one of the plurality of logic switch circuits does not carry data in order to configure the at least some of said plurality of second switch circuits as n logical switch circuits, where n is a power of 2 (*col. 5, lines 49-50, Zola discusses the*

output terminals of input stage switches 102-104 are connected to two center stage switches 201-201 (2 is a power of 2), while center stage switch 203 is available).

Regarding **claim 18**, in addition to features recited in base claim 16, Zola further discloses wherein each of said plurality of first and third switch circuits are configured to be logically represented as respective grouping of 2x2 switches (*see Fig. 4. It is noted that this limitation is a common in Clos network*).

Regarding **claim 19**, in addition to features recited in base claim 16, Zola further discloses wherein each of said plurality of outputs of said plurality of first switch circuits, outputs a respective one of a plurality of data signals, said data signals being time-division multiplexed (*Fig. 4 and col. 5, line 35-37*).

Regarding **claim 23**, in addition to features recited in base claim 16, Zola further discloses wherein each of said plurality of outputs of said plurality of switch circuits, outputs a respective one of a plurality of data signals, said data signals being multiplexed (*Fig. 4 and col. 5, line 35-37*).

Regarding **claim 25**, in accordance with Zola reference entirety, Zola shows a rearrangeable, non-blocking, three-stage switch configured as a Clos network (Fig. 4), said switch comprising:

a plurality of physical center stage switch circuits, a number of said plurality of physical center stage switch circuits equaling N, where N is an integer other than a power of 2 (*see Fig. 4 for connection and description at col. 5, lines 43-45. Three Center Stage Switches 201-203 are provides. Thus, three is not a power of 2*);

a plurality of logical center stage switch circuits equaling N*f, where f is a number of logical center stage switch circuits per physical center stage switch circuit, wherein the plurality of physical center stage switch circuits are configured into the plurality of logical center stage switch circuits (*col. 5, line 60 to col. 6, line 22, Zola discloses the connection process for using two or more center stage switches*); and

a subset of the plurality of logical center stage switch circuits equaling n, where n is less than N*f and n is a power of 2 (*Fig. 4 shows center stage switches 201-203 and at col. 5, lines 45-52, Zola shows with certain input connections only two center stage switches 201-202 are used and 2 is a power of 2*).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

12. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zola in view of Andresen (The Looping Algorithm Extended to Base 2^t Rearrangeable Switching Networks, IEEE, pages 1057-1063, 1977) (hereinafter "Andresen").

Regarding **claim 18**, Zola discloses the features in base claim 16 (see rationales discussed above) but fails to further disclose "*wherein a Looping Algorithm is used as a control algorithm for the switch*". However, such limitation lacks thereof from Zola reference is well-known as proposed by Waksman, dubbed by Tsao-Wu and extended to the case of $m= 2^t$ in the above technical paper disclosed by Andresen.

In accordance with Andresen reference entirety, Andresen discloses control algorithm for the switch in Clos networks is Looping Algorithm to provide a routing procedure gives control data applicable to base 2^t (see abstract and thereinafter).

Thus, it would have been obvious to those skilled in the art, at the time of the invention was made, having the references of Zola and Andresen readily available, to implement the Looping Algorithm into Zola's switch to arrive the claimed invention with a motivation to provide a routing procedure gives control data applicable to base 2^t (see abstract and thereinafter).

13. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zola in view of Gao et al (UPS 5,945,922) (hereinafter "Gao").

Regarding **claim 31**, Zola discloses the claimed features of base claim 25 (see rationales discussed above), but fails to further disclose "*wherein each of the plurality of physical center stage switch circuits is comprised of a second three-stage switch*". However, such limitation lacks thereof from Zola is well known and disclosed by Gao.

In accordance with Gao reference entirety, Gao discloses a widesense nonblocking switching networks (WNSN) comprising, among other things, the limitation of "*wherein each of the plurality of physical center stage switch circuits is comprised of a second three-stage switch*" (see Fig. 2; element 220) to provide multirate widesense nonblocking switching networks.

It would have been obvious to those skilled in the art at the time of the invention was made having the references readily available to incorporate Gao's WNSN into Zola's network to arrive the claimed invention with a motivation to provide multirate widesense nonblocking switching networks ('922, col. 2, lines 54-60).

Examiner's Comments

14. As for claims 27-30 and 32-33 due to the 112, first paragraph rejection above, there is no art applied to determine the allowability of the claimed invention at this time.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sahman et al (USP 6,693,902).

Yang et al (USP 5,451,936).

Hunter (USP 5,390,178) ;

Hwang, Control Algorithm for Rearrangeable Clos Networks, IEEE, pages 952-954, 1983.

Ohta, A Simple Control Algorithm for Rearrangeable Switching Networks with Time Division Multiplexed Links, IEEE, pages 1302-1308, 1987.

Jajszczyk, A Simple Algorithm for the Control of Rearrangeable Switching Networks, IEEE, pages 169-171, 1985.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Frank Duong whose telephone number is 571-272-3164. The examiner can normally be reached on 7:00AM-3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema S. Rao can be reached on 571-272-3174. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Frank Duong
Primary Examiner
Art Unit 2666

March 08, 2005